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10/801,503	03/15/2004	Guido Gabriele Albasini	2110-111-03	1822

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EXAMINER	
TRAN, KHANH C	
ART UNIT	**PAPER NUMBER**
2611	
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01/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,503	ALBASINI ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,10,11,13,16,19,23 and 24* is/are rejected.

7)☒ Claim(s) *4-9,12,14,15,17,18 and 20-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 10/22/2007 has been entered. Claims 1-24 are pending in this Office action.

Response to Arguments

2. Applicant's arguments with respect to claims 1-24 have been considered but are moot in view of the new ground(s) of rejection.

3. Objection to the Drawings has been withdrawn after Applicants clarified the claimed subject matter in claim 11.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 11, 13, 19 and 23-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Oishi et al. U.S. Patent 6,317,476 B1.

Regarding claim 11, in column 2 lines 20-45, Oishi et al. discloses FIG. 2 prior art of a fractional-N-frequency synthesizer. The fractional-N-frequency synthesizer includes

an accumulator 7 and a spurious suppressing circuit 8 newly provided in addition to the configuration of the PLL-frequency synthesizer shown in FIG. 1. The accumulator 7 receives the reference frequency fr from the frequency divider 6 as a clock frequency, and obtains a sum of an accumulated value acm and input data F at each phase-comparison cycle employed by the phase comparator 1. The accumulated value acm of the accumulator 7 is updated with an increment equal to F at each phase-comparison cycle in this manner. In light of that, input data F corresponds to the claimed first data set, an accumulated value acm corresponds to the claimed phase error value and sum of an accumulated value acm corresponds to the claimed second data set.

In column 3 lines 25-35, the spurious signal suppressing circuit 8 includes a D/A converter 9, which receives the accumulated value acm of the accumulator 7, and converts it to an electric-current signal so as to supply an output current Iad. In light of that, the spurious signal suppressing circuit 8 corresponds to the claimed generator.

Regarding claim 13, as recited in claim 11 rejection, the accumulator 7 updates the accumulated value acm with an increment equal to F at each phase-comparison cycle in this manner. In view of that, accumulator 7 corresponds to the claimed first modifier and the updated accumulated value acm corresponds to the claimed third data set.

Regarding claim 19, claims are rejected on the same ground as for claim 11 because of similar scope.

Regarding claims 23-24, claims are rejected on the same ground as for claim 11 because of similar scope.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oishi et al. U.S. Patent 6,317,476 B1 in view of Park U.S. Patent 6,219,397 B1.

Regarding claim 1, in column 2 lines 20-45, Oishi et al. discloses FIG. 2 prior art of a fractional-N-frequency synthesizer. The fractional-N-frequency synthesizer includes an accumulator 7 and a spurious suppressing circuit 8 newly provided in addition to the configuration of the PLL-frequency synthesizer shown in FIG. 1. The accumulator 7 receives the reference frequency fr from the frequency divider 6 as a clock frequency, and obtains a sum of an accumulated value acm and input data F at each phase-comparison cycle employed by the phase comparator 1.

FIG. 2 prior art discussed in Oishi et al. invention employs an accumulator 7, but does not teach utilization a sigma delta modulator.

As known in the art, sigma delta modulator can be implemented using accumulators as taught in FIG. 1 of Park teachings (see also column 4 lines 45-60). As further disclosed in column 3 lines 10-40 of Oishi et al. invention, FIG. 2 prior art

discusses a mere addition of the accumulator 7 to the PLL-frequency synthesizer is known to result in "spurious signals" being generated and provides a spurious signals suppressing circuit 8 to solve that problem. However, in column 4 lines 5-15, The fractional-N-frequency synthesizer in FIG. 2 further suffers a channel dependency of spurious signals means that a spurious signal-suppression effect by the spurious signal suppressing circuit 8 will be affected when the frequency-division ratio N of the frequency divider 5 is changed to a new ratio with an aim of switching a frequency generated by the fractional-N-frequency synthesizer. Because Park teachings employ a higher-order discrete sigma-delta modulator in the fractional-N frequency synthesizer to suppress fractional spurs (see column 2 lines 30-40), one of ordinary skill in the art at the time the invention was made would have been motivated to modify the accumulator 7 to implement the higher-order discrete sigma-delta modulator 170 (FIG. 1) as taught by Park.

Referring back to FIG. 2 of Oishi et al. invention, dividing ratio of frequency divider 5 changes from n to N+1; see column 3 lines 45-55. The accumulated value acm accumulated of the accumulator 7 is updated with an increment equal to F at each phase-comparison cycle according Sov and the spurious signals suppressing circuit 8 calculates a correction value to condition a control signal (output from charge pump circuit 2 in FIG. 2).

Regarding claim 2, as recited in claim 1 rejection, Park teachings employ a higher-order discrete sigma-delta modulator in the fractional-N frequency synthesizer.

Regarding claim 3, as further shown in FIG. 1, Park higher-order discrete sigma-delta modulator is multi-bit modulator.

Regarding claim 10, claim is rejected on the same ground as for claim 1 because of similar scope.

6. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Oishi et al. U.S. Patent 6,317,476 B1.

Regarding claim 16, in column 3 lines 20-35, see also FIG. 2, Oishi et al. discloses the spurious signal suppressing circuit 8 includes a D/A converter 9, which receives the accumulated value acm of the accumulator 7, and converts it to an electric-current signal so as to supply an output current Iad.

The spurious signal suppressing circuit 8 includes a D/A converter 9, but does not show a first modifier as claimed in the application claim.

Nevertheless, because the spurious signal suppressing circuit 8 is to suppress spurious signals, one of ordinary skill in the art at the time the invention was made would have recognized that the spurious signal suppressing circuit 8 would further include other processing components (does not show in the FIG.) before D/A converter 9 to perform the suppression.

Allowable Subject Matter

7. Claims 4-9, 12, 14-15, 17-18 and 20-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Castiglione et al. U.S. Patent 7,079,616 B2.

Hietala U.S. Patent 5,495,206.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on 571-272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Cong Tran

KHANH C. TRAN
PRIMARY EXAMINER

1/16/2008
AU 2611